

NP100N04NUJ

MOS FIELD EFFECT TRANSISTOR

R07DS0364EJ0100 Rev.1.00 Jun 13, 2011

Description

The NP100N04NUJ is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
 - $R_{DS(on)} = 3.0 \text{ m}\Omega \text{ MAX}.$ ($V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$)
- Low C_{iss} : $C_{iss} = 5600 \text{ pF TYP}$. $(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V})$
- High current rating: $I_{D(DC)} = \pm 100 \text{ A}$
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

| Part No. | Lead Plating | Packing | Package |
|-----------------------|---------------|----------------|----------------------------|
| NP100N04NUJ-S18-AY *1 | Pure Sn (Tin) | Tube 50 p/tube | TO-262 (MP-25SK) TYP. 1.8g |

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings ($T_A = 25$ °C)

| Item | Symbol | Ratings | Unit |
|-------------------------------------------------|-----------------------|-------------|----------|
| Drain to Source Voltage (V _{GS} = 0 V) | V_{DSS} | 40 | V |
| Gate to Source Voltage (V _{DS} = 0 V) | V_{GSS} | ±20 | V |
| Drain Current (DC) (T _C = 25°C) | I _{D(DC)} | ±100 | Α |
| Drain Current (pulse) *1 | I _{D(pulse)} | ±400 | Α |
| Total Power Dissipation (T _C = 25°C) | P _{T1} | 220 | W |
| Total Power Dissipation (T _A = 25°C) | P _{T2} | 1.8 | W |
| Channel Temperature | T _{ch} | 175 | °C |
| Storage Temperature | T _{stg} | −55 to +175 | °C |
| Repetitive Avalanche Current *2 | I _{AR} | 60 | Α |
| Repetitive Avalanche Energy *2 | E _{AR} | 360 | mJ |

Thermal Resistance

Channel to Case Thermal Resistance $R_{th(ch-C)}$ 0.68 °C/W Channel to Ambient Thermal Resistance *2 $R_{th(ch-A)}$ 83.3 °C/W

Notes: *1. T_C = 25°C, PW \leq 10 μ s, Duty Cycle \leq 1%

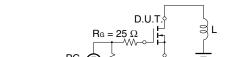
*2. $T_{ch(peak)} \le 150^{\circ}C$, $R_G = 25 \Omega$

Electrical Characteristics (T_A = 25°C)

| Item | Symbol | MIN. | TYP. | MAX. | Unit | Test Conditions |
|-------------------------------------------|---------------------|------|------|------|------|---------------------------------------------------|
| Zero Gate Voltage Drain Current | I _{DSS} | | | 1.0 | μΑ | $V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$ |
| Gate Leakage Current | I _{GSS} | | | ±100 | nA | $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$ |
| Gate to Source Threshold Voltage | $V_{GS(th)}$ | 2.0 | 3.0 | 4.0 | V | $V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$ |
| Forward Transfer Admittance *1 | y _{fs} | 45 | 87 | | S | $V_{DS} = 5 \text{ V}, I_{D} = 50 \text{ A}$ |
| Drain to Source On-state Resistance *1 | R _{DS(on)} | | 2.5 | 3.0 | mΩ | V _{GS} = 10 V, I _D = 50 A |
| Input Capacitance | C _{iss} | | 5600 | 8400 | pF | $V_{DS} = 25 V$, |
| Output Capacitance | Coss | | 920 | 1380 | pF | $V_{GS} = 0 V$, |
| Reverse Transfer Capacitance | C _{rss} | | 340 | 620 | pF | f = 1 MHz |
| Turn-on Delay Time | t _{d(on)} | | 25 | 60 | ns | $V_{DD} = 20 \text{ V}, I_D = 50 \text{ A},$ |
| Rise Time | t _r | | 15 | 40 | ns | $V_{GS} = 10 V$, |
| Turn-off Delay Time | $t_{d(off)}$ | | 93 | 190 | ns | $R_G = 0 \Omega$ |
| Fall Time | t _f | | 13 | 40 | ns | |
| Total Gate Charge | Q_G | | 110 | 170 | nC | $V_{DD} = 32 \text{ V},$ |
| Gate to Source Charge | Q _{GS} | | 22 | | nC | $V_{GS} = 10 \text{ V},$ |
| Gate to Drain Charge | Q_{GD} | | 32 | | nC | I _D = 100 A |
| Body Diode Forward Voltage *1 | $V_{F(S-D)}$ | | 0.9 | 1.5 | V | I _F = 100 A, V _{GS} = 0 V |
| Reverse Recovery Time | t _{rr} | | 55 | | ns | I _F = 100 A, V _{GS} = 0 V, |
| Reverse Recovery Charge | Q _{rr} | | 77 | | nC | di/dt = 100 A/μs |

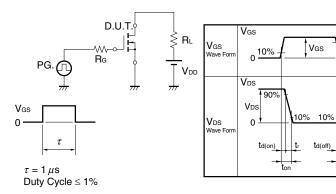
Note: *1. Pulsed test

TEST CIRCUIT 1 AVALANCHE CAPABILITY



Starting Tch

TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

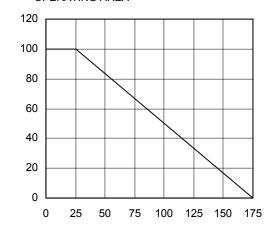
$$\begin{array}{c|c} D.U.T. \\ I_G = 2 \underbrace{mA}_{W} & \\ \hline \\ PG. & \\ \hline \\ \end{array} \begin{array}{c} S & \\ S & \\ \hline \\ \end{array} \begin{array}{c} V_{DD} \\ \hline \\ \end{array}$$

90%

dT - Percentage of Rated Power - %

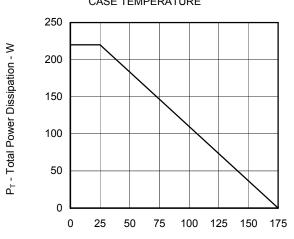
Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



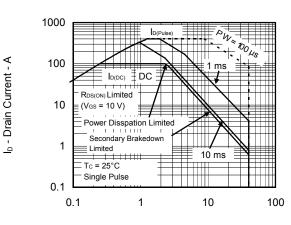
T_C - Case Temperature - °C

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



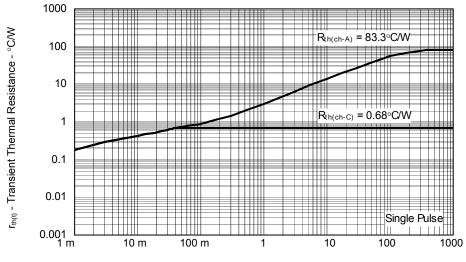
 T_{C} - Case Temperature - $^{\circ}\text{C}$

FORWARD BIAS SAFE OPERATING AREA



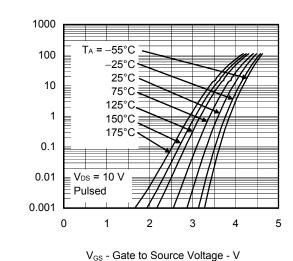
 V_{DS} - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



PW - Pulse Width - s

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE 450 400 350 I_D - Drain Current - A 300 250 200 150 100 V_{GS} = 10 V 50 Pulsed 0 0.2 0.4 0.6 8.0 1.2 V_{DS} - Drain to Source Voltage - V

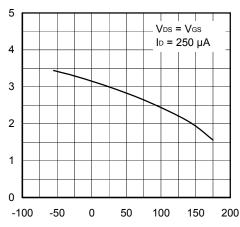


Ip - Drain Current - A

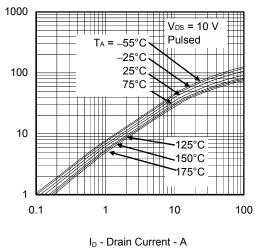
y_{fs} | - Forward Transfer Admittance - S

FORWARD TRANSFER CHARACTERISTICS

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

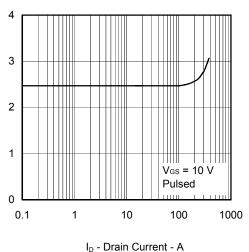


FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

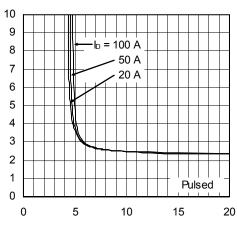


T_{ch} - Channel Temperature - °C

DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



V_{GS} - Gate to Source Voltage - V

 $R_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $\mathfrak{m}\Omega$

 $R_{DS(on)}$ - Drain to Source On-state Resistance - $m\Omega$

V_{GS(th)} - Gate to Source Threshold Voltage - V

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

t_{d(on)}, t_r, t_{d(off)}, t_f - Switching Time - ns

IF - Diode Forward Current - A

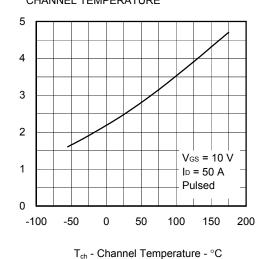
Crss

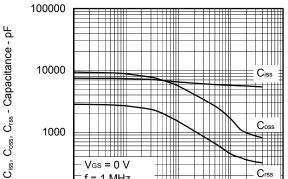
11111

100

10

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE





Vgs = 0 V

f = 1 MHz

0.1

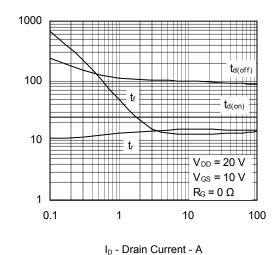
100

0.01

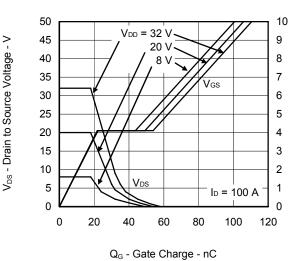
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

V_{DS} - Drain to Source Voltage - V

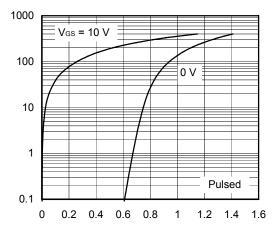
SWITCHING CHARACTERISTICS



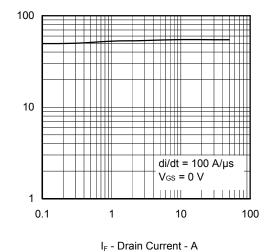
DYNAMIC INPUT/OUTPUT CHARACTERISTICS







SOURCE TO DRAIN DIODE FORWARD VOLTAGE

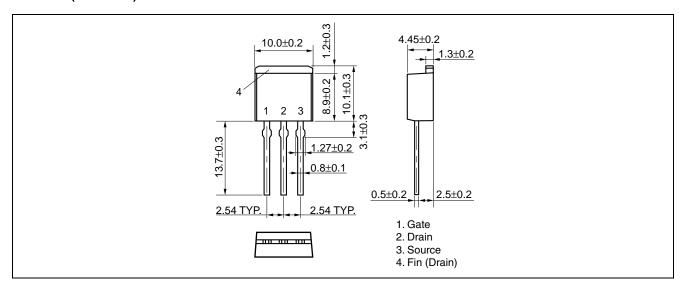


 $V_{F(S-D)}$ - Source to Drain Voltage - V

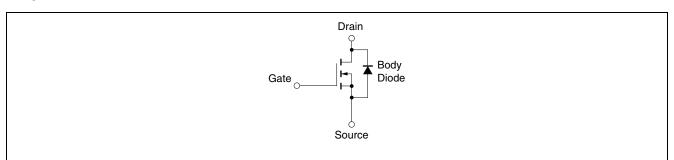
t_{rr} - Reverse Recovery Time - ns

Package Drawings (Unit: mm)

TO-262 (MP-25SK)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History

NP100N04NUJ Data Sheet

| | | Description | | |
|------|--------------|-------------|----------------------|--|
| Rev. | Date | Page | Summary | |
| 1.00 | Jun 13, 2011 | _ | First Edition Issued | |

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